WHAT IS CLAIMED IS:

1. In a ROM device using a plurality of data resistors to interconnect a plurality of input word lines with a plurality of output bit lines, a temperature compensation circuit to maintain a current through a selected one of said data resistors substantially constant comprising:

at least one reference resistor, wherein the conductivity of said reference resistors is responsive to changes in temperature;

a constant current source coupled to said at least one reference resistor, said constant current source developing a voltage across said at least one reference resistor; and

at least one switch connected to said at least one reference resistor to selectively couple said voltage to said input word lines.

2. A temperature compensation circuit as recited in Claim 1 wherein conductive properties of said reference resistor are selected to be the same as the conductive properties of said data resistors.

3. A temperature compensation circuit as recited in Claim 2 wherein said data resistor is selected from a polysilicon material.

4. A temperature compensation circuit as recited in Claim 3 wherein said polysilicon material is undoped.

5. A temperature compensation circuit as recited in Claim 3 wherein said polysilicon material is doped.

6. A temperature compensation circuit as recited in Claim 2 wherein said data resistor is comprised of a metal oxide.

7. A temperature compensation circuit as recited in Claim 1 wherein conductive properties of said reference resistors are selected to be substantially similar to the conductive properties of said data resistors.

8. A temperature compensation circuit as recited in Claim 7 wherein said data resistor is selected from a polysilicon material.

9. A temperature compensation circuit as recited in Claim 8 wherein said polysilicon material is undoped.

10. A temperature compensation circuit as recited in Claim 8 wherein said polysilicon material is doped.

11. A temperature compensation circuit as recited in Claim 7 wherein said data resistor is comprised of a metal oxide.

12. A temperature compensation circuit as recited in Claim 1 further comprising:

a plurality of sense amplifiers coupled to said output bit lines, each output line having at least one sense amplifier, said sense amplifier receiving said constant current flowing through said data resistors wherein each of said sense amplifier provides a constant output voltage.

13. A temperature compensation circuit as recited in Claim 12 wherein said sense amplifier comprises

an operational amplifier with a fixed feedback resistor, R, wherein said amplifier output voltage is determined from the value of said constant current and said feedback resistor.

14. A temperature compensation circuit as recited in Claim 13 wherein said feedback resistor is temperature independent.

15. A temperature compensation circuit as recited in Claim 1 wherein said at least one switch selectively couples said voltage to a selected one of said input word lines when an input to said switch is high.

16. A temperature compensation circuit as recited in Claim 1 wherein said at least one switch selectively couples said voltage to a selected one of said input word lines when an input to said switch is low.

17. A temperature compensation circuit as recited in Claim 12 wherein said sense amplifier is operated in the non-linear region.

18. A temperature compensation circuit as recited in Claim 12 wherein said sense amplifier is operated in the linear region.

19. A method to maintain a current through Read-Only Memory (ROM) substantially constant as temperature changes wherein said ROM employs a plurality of data resistors to provide electrical interconnections between a plurality of input lines and output lines, comprising the steps of:

selecting a reference resistor having substantially similar properties of conductivity as said data resistor;

supplying a reference voltage to said input lines, said reference voltage developed by supplying a constant current to said reference resistor, wherein said reference voltage is responsive to a change in temperature.

20. The method as recited in Claim 19 wherein said data resistor is comprised of undoped polysilicon.

21. The method as recited in Claim 19 wherein said data resistor is comprised of doped polysilicon.

22. The method as recited in Claim 19 wherein the step of supplying said reference voltage further comprises the step of selectively switching said reference voltage to said word line.

23. In a ROM device using a plurality of data resistors to interconnect a plurality of input word lines with a plurality of output bit lines, a temperature compensation circuit to maintain a current through a selected one of said data resistors substantially constant comprising:

at least one voltage source producing a voltage that is responsive to changes in temperature; and

at least one switch connected to said at least one voltage source to selectively couple said voltage to said input word lines.

24. A temperature compensation circuit as recited in Claim 23 further comprising:

a plurality of sense amplifiers coupled to said output bit lines, each output line having at least one sense amplifier, said sense amplifier receiving said

constant current flowing through said data resistors wherein each of said sense amplifier provides a constant output voltage.

25. A temperature compensation circuit as recited in Claim 24 wherein said sense amplifier comprises

an operational amplifier with a fixed feedback resistor, R, wherein said amplifier output voltage is determined from the value of said constant current and said feedback resistor.

26. A temperature compensation circuit as recited in Claim 25 wherein said feedback resistor is temperature independent.

27. A temperature compensation circuit as recited in Claim 24 wherein said sense amplifier is operated in the non-linear region.

28. A temperature compensation circuit as recited in Claim 24 wherein said sense amplifier is operated in the linear region.

29. A temperature compensation circuit as recited in Claim 23 wherein said at least one switch selectively couples said voltage to a selected one of said input word lines when an input to said switch is high.

30. A temperature compensation circuit as recited in Claim 23 wherein said at least one switch selectively couples said voltage to a selected one of said input word lines when an input to said switch is low.

31. A temperature compensation circuit as recited in claim 23 wherein said temperature responsive voltage changes to compensate for changes in voltage across said data resistor.

32. A method to maintain a current through Read-Only Memory (ROM) substantially constant as temperature changes wherein said ROM employs a plurality of data resistors to provide electrical interconnections between a plurality of input lines and output lines, comprising the steps of:

supplying a reference voltage that is responsive to changes in temperature to said input lines, wherein said reference voltage changes to maintain said current through said data resistor substantially constant.

33. The method as recited in Claim 32 wherein the step of supplying said reference voltage further comprises the step of selectively switching said reference voltage to said word line.